stub interrupt, executing said main interrupt handling routine, resuming execution of said stub interrupt handling routine and resuming data operations. Processing logic was not rejected by this Examiner as not being enabled in the originally filed application and thus it is taken as admitted that processing logic was enabled. As confirmed by the Manual of Patent Examining Procedure (MPEP) §2164.01, "[t]he standard for determining whether the specification meets the enablement requirement was . . . is the experimentation needed to practice the invention undue or unreasonable?" The Examiner apparently answered this question in the negative in holding that the originally filed claims were enabled by the originally filed specification.

The MPEP at §2173.05(e) also clearly states that "[i]nherent components of elements recited have antecedent basis in the recitation of the components themselves. For example, the limitation 'the outer surface of said sphere' would not require an antecedent recitation that the sphere has an outer surface." Thus it would be readily apparent to one of ordinary skill that if an apparatus could perform logic functions, there would be some structure for performing those functions.

Applicants' specification, page 12, line 30, describes the data processing apparatus including a processor core 10. Those of ordinary skill in the art will be well aware that processing cores include programmable circuitry for performing various logical functions. It would be abundantly clear to those persons of ordinary skill in this art that the processor core circuitry is known to perform various steps and Applicants have merely modified claim 7 to specifically recite circuitry for performing the recited logical steps. Because the original claim specifies processing logic implemented in an apparatus for processing data, there is clear

antecedent basis for the specific circuitry for performing the recited logical steps of claim 7 and no further disclosure in the specification is necessary.

It is also noted that if the originally recited processing logic steps were supported by the specification (and Applicants strongly contend that they are and notes that there was no PTO objection to this language previously), then the specification inherently provides enablement support for the apparatus for processing data having the individually recited circuitries for accomplishing the logical steps.

Accordingly, reconsideration of the rejection of claim 7 under 35 USC §112 (first paragraph) is respectfully requested.

Applicants have conducted a detailed review of all of the Examiner's arguments regarding the application of the Saito reference to claims pending in the current application, including the Examiner's recently added "Response to Arguments" portion. The Examiner, as noted in Applicants' previously filed Amendment, commits numerous errors, the primary error of which is his failure to direct attention to the language of Applicants' claims and the fact that the Saito reference does not disclose or render obvious the subject matter of the claims, and instead seems to be distracted by similar, but non-claimed features. Applicants will summarize the Examiner's errors as follows.

Error #1. The Examiner errs in suggesting that Saito Figure 5 element 123 and paragraph 82 contain any disclosure of Applicants' claimed "as commanded by said stub interrupt handling routine, suspending execution . . ." step

On page 4, lines 1-3, the Examiner alleges that the third step of Applicants' independent claim 1 (beginning "as commanded by said stub interrupt handling routine, . . .") is somehow disclosed in Saito's Figure 5 by element 123 as discussed in paragraph 82.

In looking at the entirety of Saito's paragraph 82, there are discussions about "normalized priorities" and the "priority translation modules 122 and 123" and the fact that there is a "priority comparison" and a statement that the "normalized priorities 172 and 173 take the values of 124 and 255 respectively." However, there is no suggestion in Saito's paragraph 82 that either priority translation modules 122 and 123 are disclosing "suspending a stub interrupt handling routine" or "starting execution of an interrupt handling routine." In fact, nothing in Saito's paragraph 82 has anything to do with Applicants' claimed third method step of "suspending execution of said stub interrupt handling routine and starting a main interrupt handling routine executing under control of said second operation system."

Accordingly, the Examiner clearly fails to meet his burden of establishing a *prima facie* case of anticipation because this claimed method step (or the corresponding apparatus elements in independent apparatus claim 7) is not disclosed in Saito. Should the Examiner believe otherwise, he is respectfully requested to specifically identify any teaching in Saito which he contends corresponds to Applicants' claim 1, third step (or the corresponding structure in claim 7). Absent any specific teaching, the Examiner's anticipation rejection of claims 1 and 7 respectfully traversed.

Error #2. The Examiner repeatedly errs in citing paragraph 63 of Saito as allegedly teaching portions of claim 1 (see paragraphs 2, 3 and 4 on page 4 of the Official Action)

In paragraphs 2-4 on page 4 of the Final Rejection, the Examiner contends that Saito's paragraph 63 and Figure 6 disclose the subject matter as set out in Applicants' independent claim 1, paragraphs 4, 5 and 6 (and the corresponding paragraphs in independent claim 7). Again, the error of the Examiner's position is clearly obvious by reviewing paragraph 63 of the Saito reference. There is no disclosure of "executing" a main interrupt handling routine or "resuming execution of said stub interrupt handling routine" or "resuming said data processing operations" as specified in independent claim 1, paragraphs 4, 5 and 6 (and the corresponding elements in claim 7).

In order to support an anticipation rejection, there must be at least one colorable disclosure of Applicants' claimed method step contained in the cited prior art reference. In fact, in order to anticipate a method claim, all of the claimed method steps must be disclosed in a single reference and all claimed interrelationships between the method steps must also be disclosed. If the Examiner cannot establish where Applicants' claimed method steps (or the corresponding apparatus elements of apparatus claim 7) are disclosed in the single Saito reference, he simply fails to meet his burden of establishing any anticipation of the claims.

The Examiner's attention is directed towards the case of *Lindemann Maschinenfabrik GMBH v. American Hoist & Derrick*, 221 USPQ 481, 485 (Fed. Cir. 1984) in which the Court of Appeals for the Federal Circuit held that " a]nticipation requires the presence in a single prior art reference disclosure of each and every element of the claimed invention, arranged as in the claim."

Thus, because of the errors noted above, the Final Rejection does not establish any *prima facie* case of "anticipation" because the Rejection fails to identify where any single prior art document teaches each and every method step and each and every claimed interrelationship between method steps as required by Applicants' independent claim 1 or the apparatus elements and the interrelationship between the apparatus elements as set out in independent claim 7. Accordingly, claims 1 and 7 and claims dependent thereon are clearly patentable over the Saito reference because of the Examiner's failure to meet his burden of establishing that Saito teaches the claimed steps and elements.

The Examiner, in section 9 on pages 7 and 8 of the Final Rejection, attempts to respond to the previous arguments of patentability over the Saito reference. However, he does not cure the above deficiencies by indicating where the claimed method steps and apparatus elements are shown in the Saito or Worley references. Applicants will respond to the various errors contained in this discussion.

Error #3. The Examiner again reiterates that he believes that Saito teaches the claimed step of "suspending execution of said stub interrupt handling program and starting a main interrupt handling routine executing under control of said second operating system"

The Examiner here goes off on a tangent in terms of support for an "anticipation" rejection that simply has no basis in §102. The Examiner compares some **unclaimed** structures of Applicants' preferred embodiment of the claimed invention and some aspects of the Saito document. Importantly, the Examiner's comparison involves **unclaimed subject matter**, i.e., "priority" and possible interrupt handling system priority, and fails to identify any teaching in

Saito of the **claimed** subject matter. A brief review of independent claims 1 and 7 and then a comparison with the Saito disclosure indicates that in the claims there is no mention of "priority" or "interrupt priority." Therefore, whether or not Saito teaches "priority" or "interrupt priority" is irrelevant because this is not claimed in claims 1 and 7 and thus is irrelevant to the issue of where Saito teaches the claimed method steps and/or apparatus elements.

Again, it would appear that the Examiner is attempting to use any perceived similarity (as opposed to the claimed steps and elements) between the present invention and the prior art as a basis for rejection. The Examiner is reminded that the only basis for rejection under §102 is whether the prior art contains a disclosure of each of the method steps and apparatus elements and their claimed interrelationship. The Examiner's reliance upon a similarity between Saito and the claimed invention involving the unclaimed "priority" or "interrupt priority" is misguided at best.

Error #4. On page 7, section 9, subsection a, the Examiner erroneously relies upon Saito's paragraphs 63 and 140

In section 9a on page 7, the Examiner references Saito's priority translation modules 122 and 123 in paragraph 63 and priority reverse translation tables 282 and 283 in paragraph 140 as allegedly disclosing "priorities." However, Applicants' independent claims 1 and 7 do not claim "priority," "priority translation modules" or "priority reverse translation tables." As a result, even assuming that the Saito reference does teach the "priority" related steps and structures, paragraphs 63 nor 140 are not even alleged to teach the limitations of Applicants' independent claims 1 and 7 and therefore any further rejection based thereon is respectfully traversed.

Error #5. The Examiner misinterprets Saito's paragraph 85 which clearly fails to teach a "stub interrupt handling routine" and/or a "starting a main interrupt handling routine"

The Examiner's reference to Saito's paragraph 85 and Figure 6 in his discussion on page 7 of the Final Rejection is taken as a suggestion that this paragraph contains some teaching of Applicants' claimed subject matter. Again, Applicants can find no disclosure in Saito's Figure 6 or paragraph 85 which discloses claim 1's third step, i.e., "suspending execution of said stub interrupt handling routine and starting a main interrupt handling routine executing under control of said second operating system."

Should the Examiner contend that this is disclosed in some portion of Saito, he is again respectfully requested to identify exactly what language exists in Saito and how he believes this language anticipates the claim language, i.e., "suspending execution . . ." for independent claims 1 and 7. Absent any specific reference, it is clear that the Examiner has failed to meet the burden of establishing anticipation under 35 USC §102.

Error #6. The Examiner, in his Response to Arguments, erroneously suggests that there is some correspondence between a "priority translation module" in Saito and the claimed "stub interrupt handling routine" recited in Applicants' independent claims 1 and 7

The Examiner appears to try to justify his discussion of "priority translation module" and "priority translation table" as being associated with "an operating system." The Examiner then appears to suggest that because these priority related modules are associated with an operating system, they somehow disclose Applicants' claimed method of processing data with execution of data processing operations under control of either a first operating system or a second operating system.

In the Saito system, the operating system that runs is set by task priority (see Saito paragraph 108). The operating system of Saito on which the interrupt is run is set by the common interrupt handler (see Saito paragraph 105). Saito neither discloses nor suggests that an interrupt under one operating system (e.g., handler 152 of Figure 10 in Saito) starts an interrupt under the other operating system (handler 153 of Figure 10).

Moreover, it is clear that none of the cited paragraphs of Saito disclose Applicants' claimed method step of "suspending execution of said stub interrupt handling routine and starting a main interrupt handling routine executing under control of said second operating system" or any of the other features of independent claims 1 and 7.

Again, the Examiner is challenged to identify specifically where the claimed method steps and apparatus elements are disclosed in Saito. Absent any corresponding disclosure of claimed method steps and apparatus elements in Saito, there is simply no basis for any further rejection under 35 USC §102.

Error #7. The Examiner appears to misunderstand his burden of proving anticipation and/or obviousness

Towards the end of paragraph 9a on page 7, the Examiner states that "Applicant is reminded that rejections are based on references as a whole and not just the cited passages. Although the specified citations are representative of the teachings in the art and are applied to specific limitations within the individual claim, other passages and figures may apply as well." The Examiner is simply incorrect in this assessment.

As noted above, the Court of Appeals for the Federal Circuit has held that, to prove anticipation, the single reference must show each and every claimed element and claimed

interrelationship. The Court has also held that "the PTO has the burden under Section 103 to establish a *prima facie* case of obviousness." *In re Fine*, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988). "It can satisfy this burden only by showing some objective teaching in the prior art or that knowledge generally available to one of ordinary skill in the art would lead that individual to combine the relevant teachings of the references."

Because the Examiner has failed to demonstrate where any one of the references teach the method steps of claim 1 or the apparatus elements of independent claim 7 or claims dependent thereon, there can be no *prima facie* case of anticipation.. Similarly, because claimed method steps and claimed apparatus elements are missing from all of the cited references, not only is there no anticipation, but the Examiner has also failed to meet his burden of establishing a *prima facie* case of obviousness.

There has been no allegation that either Saito or Worley disclose the claimed features of Applicants' independent claims or claims dependent thereon. There is simply no statute, judicial decision, rule or burden on the Applicants to prove a negative, i.e., to go through each cited references in a vain attempt to prove that no reference has any support for the Examiner's rejection. As noted above, the Court's have held that this is the Examiner's job and, if he cannot find disclosure of all claimed elements in a single reference, he cannot support a rejection under 35 USC §102. Similarly, if the Examiner cannot find support for all claimed elements among several references and if he has not expressed a basis or rationale for combining those references, he cannot establish a *prima facie* case of obviousness under 35 USC §103.

In view of the above discussion, th re is no basis for rejection of claims 1 and 7 and claims dependent thereon under 35 USC § 02 or §103, as the Examiner has completely failed to establish any *prima facie* case.

Having responded to all objection and rejections set forth in the outstanding Official Action, it is submitted that claims 1-13 ar in condition for allowance and notice to that effect is respectfully solicited. In the event the Ex miner is of the opinion that a brief telephone or personal interview will facilitate allowan of these claims, he is respectfully requested to contact Applicants' undersigned represen tive.

Respectfully submitted,

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